EEL 4744

Menu

- System Clock on XMEGA
  - >See HW 4 and the file clock.s (which is available as clock.s.txt).
    - – You will need this for Lab 8.

See examples on web-site:
doc8331 (section 7), ATxmega128a1udef.inc or **iox128a1u.h**

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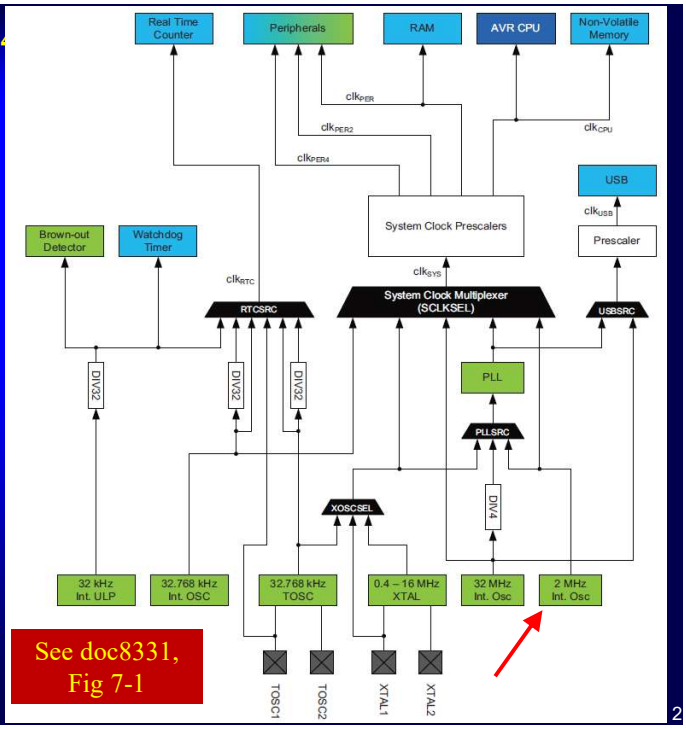
EEL 4744

XMEGA Clock System

- Read doc8331, section 7



See doc8331, Fig 7-1

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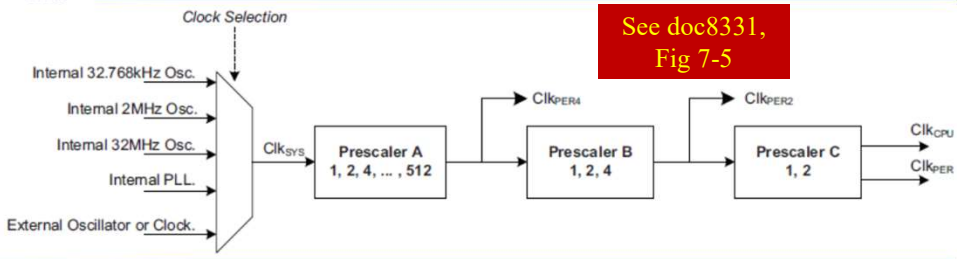
EEL 4744 System Clock Selection/Prescalers



See doc8331, Fig 7-5

- Internal **2 MHz** is the default on the XMEGA
- If want something else, usually set internal Osc to **32 MHz** and then use **Prescaler A**
  - >For 32 MHz, use the following values and registers
    - – OSC_RC32MEN_bm, OSC_CTRL, OSC_Status, OSC_RC32MRDY_bp, CCP_IOREG_gc, CPU_CCP, CLK_SCLKSEL_RC32M_gc, CLK_CTRL

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EEL 4744 Oscillator Control Register

- Enable the required oscillator in OSC_CTRL
  - >Ex: See include file
    - – OSC_RC2MEN_bm = 0x01 ; Internal 2 MHz RC Oscillator Enable bit mask
    - – OSC_RC32MEN_bm = 0x02 ; Internal 32 MHz RC Oscillator Enable bit mask
  - > **RC2MEN**: 2 MHz Internal Oscillator Enable
    - – By default, the 2 MHz internal oscillator is enabled
  - > **RC32MEN**: 32 MHz Internal Oscillator Enable
  - > **RC32KEN**: 32.768 kHz Internal Osc Enable
  - > **XOSCEN**: External Oscillator Enable
  - > **PLLEN**: PLL Enable

Normally use one of these

See doc8331, Section 7.10.1

OSC_CTRL

7	6	5	4	3	2	1	0
–	–	–	PLLEN	XOSCEN	RC32KEN	RC32MEN	RC2MEN
R	R	R	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	1

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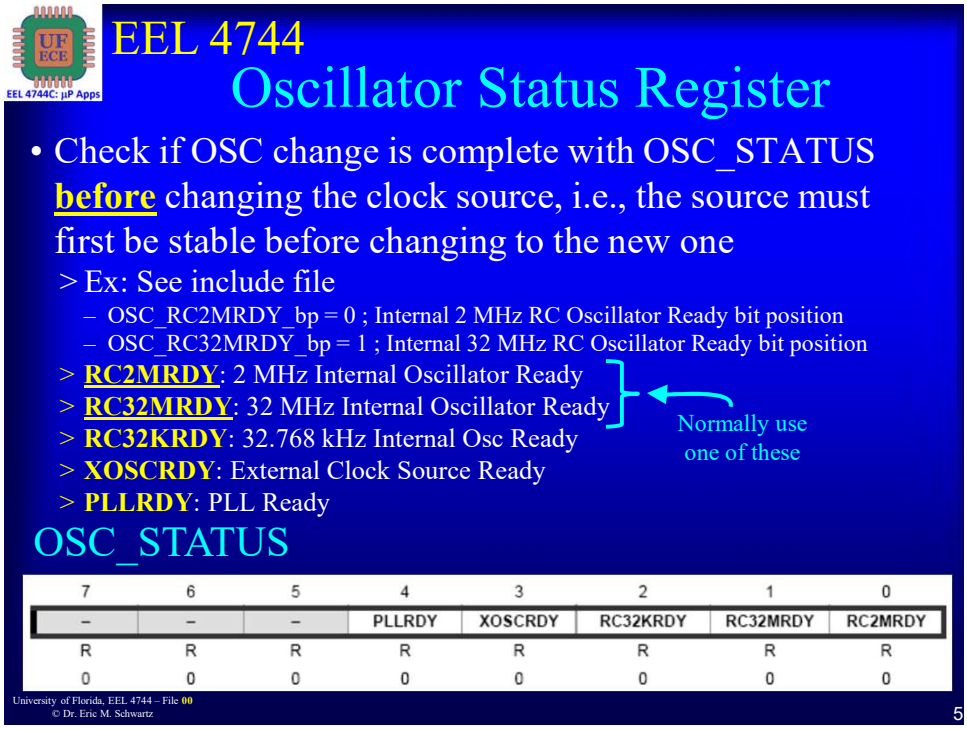
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Oscillator Status Register
• Check if OSC change is complete with OSC_STATUS before changing the clock source, i.e., the source must first be stable before changing to the new one
> Ex: See include file
– OSC_RC2MRDY_bp = 0 ; Internal 2 MHz RC Oscillator Ready bit position
– OSC_RC32MRDY_bp = 1 ; Internal 32 MHz RC Oscillator Ready bit position
> RC2MRDY: 2 MHz Internal Oscillator Ready
> RC32MRDY: 32 MHz Internal Oscillator Ready
> RC32KRDY: 32.768 kHz Internal Osc Ready
> XOSCRDY: External Clock Source Ready
> PLLRDY: PLL Ready
Normally use one of these
OSC_STATUS
7 6 5 4 3 2 1 0
– – – PLLRDY XOSCRDY RC32KRDY RC32MRDY RC2MRDY
R R R R R R R R
0 0 0 0 0 0 0 0
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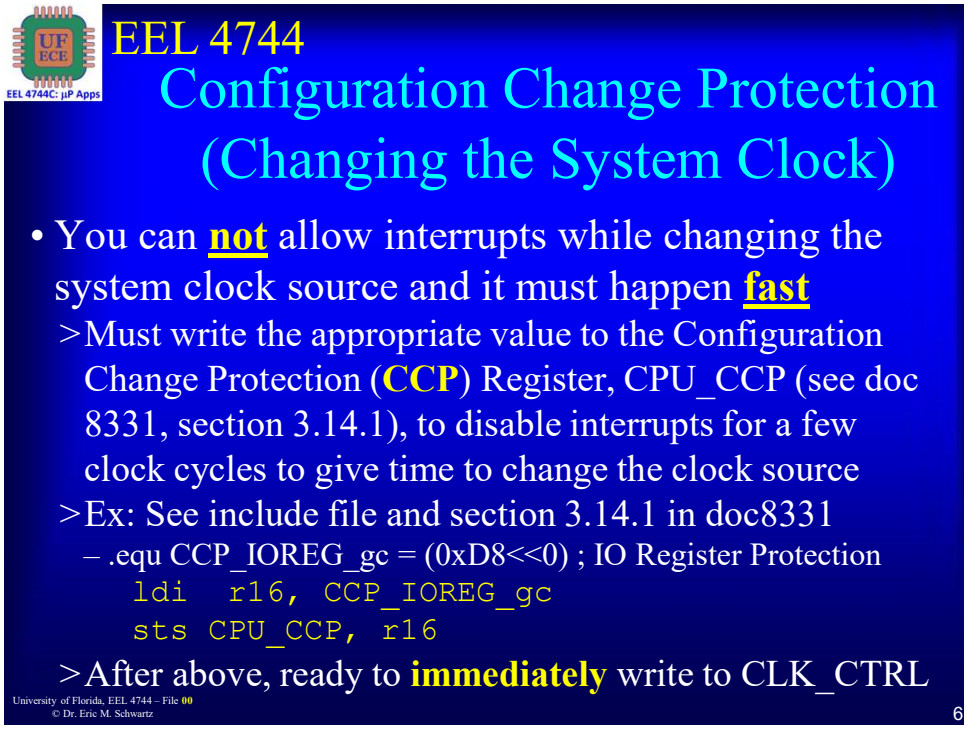
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Configuration Change Protection
(Changing the System Clock)
• You can not allow interrupts while changing the system clock source and it must happen fast
>Must write the appropriate value to the Configuration Change Protection (CCP) Register, CPU_CCP (see doc 8331, section 3.14.1), to disable interrupts for a few clock cycles to give time to change the clock source
>Ex: See include file and section 3.14.1 in doc8331
– .equ CCP_IOREG_gc = (0xD8<<0) ; IO Register Protection
ldi r16, CCP_IOREG_gc
sts CPU_CCP, r16
>After above, ready to immediately write to CLK_CTRL
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See doc8331, Section 7.9.1

Clock Control Register

- Store to CLK_CTRL to change the system clock
  - >Ex: See include file
    - – CLK_SCLKSEL_RC32M_gc = (0x01<<0) ; Internal 32 MHz RC Oscillator
    - – CLK_SCLKSEL_RC2M_gc = (0x00<<0) ; Internal 2 MHz RC Oscillator

CLKSEL [2..0]	Group Config	Description
000	RC2MHZ	2MHz int osc
001	RC32MHZ	32MHz int osc
010	RC2KHZ	32.768 int osc
011	XOSC	Ext osc
100	PLL	Phase locked loop
101	---	Reserved
11-	---	Reserved

CLK_CTRL

7	6	5	4	3	2	1	0
–	–	–	–	–	SCLKSEL[2:0]		
R	R	R	R	R	R/W	R/W	R/W
0	0	0	0	0	0	0	0

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Changing the System Clock

- Once the clock is set to 32 MHz, you can change the system clock by using CLK_PSCTRL along with CLK_PSADIV_x_gc, CLK_PSBCDIV_y_gc, where x is a power of 2 between 1 and 512 and y corresponds to a Prescaler B value and a Prescaler C value
  - >Both Prescaler B & C (PSBC) divider values are usually 1:

```
.equ CLK_PSBCDIV_1_1_gc = (0x00<<0)
        ; Divide B by 1 and C by 1
```

  - >For a Prescaler A divider value of 4 ATxmega128a1udef.inc

```
.equ CLK_PSADIV_4_gc = (0x03<<2) ; Divide by 4
```

  - – See doc8331, Table 7-2 (on next page)

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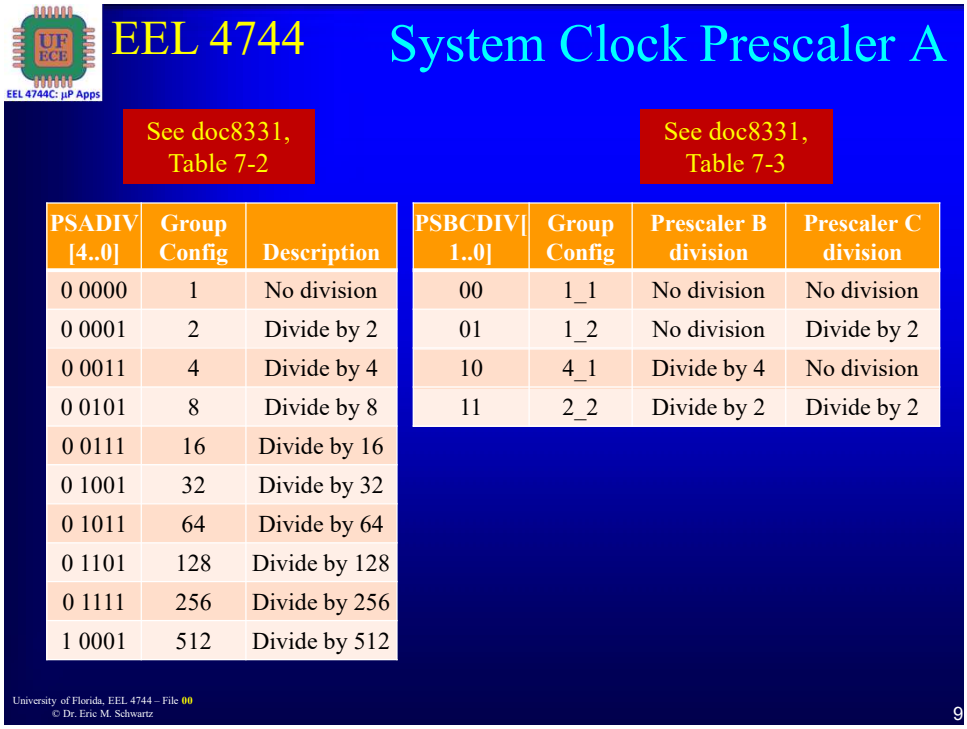

PSADIV [4..0]	Group Config	Description
0 0000	1	No division
0 0001	2	Divide by 2
0 0011	4	Divide by 4
0 0101	8	Divide by 8
0 0111	16	Divide by 16
0 1001	32	Divide by 32
0 1011	64	Divide by 64
0 1101	128	Divide by 128
0 1111	256	Divide by 256
1 0001	512	Divide by 512

PSBCDIV[1..0]	Group Config	Prescaler B division	Prescaler C division
00	1_1	No division	No division
01	1_2	No division	Divide by 2
10	4_1	Divide by 4	No division
11	2_2	Divide by 2	Divide by 2

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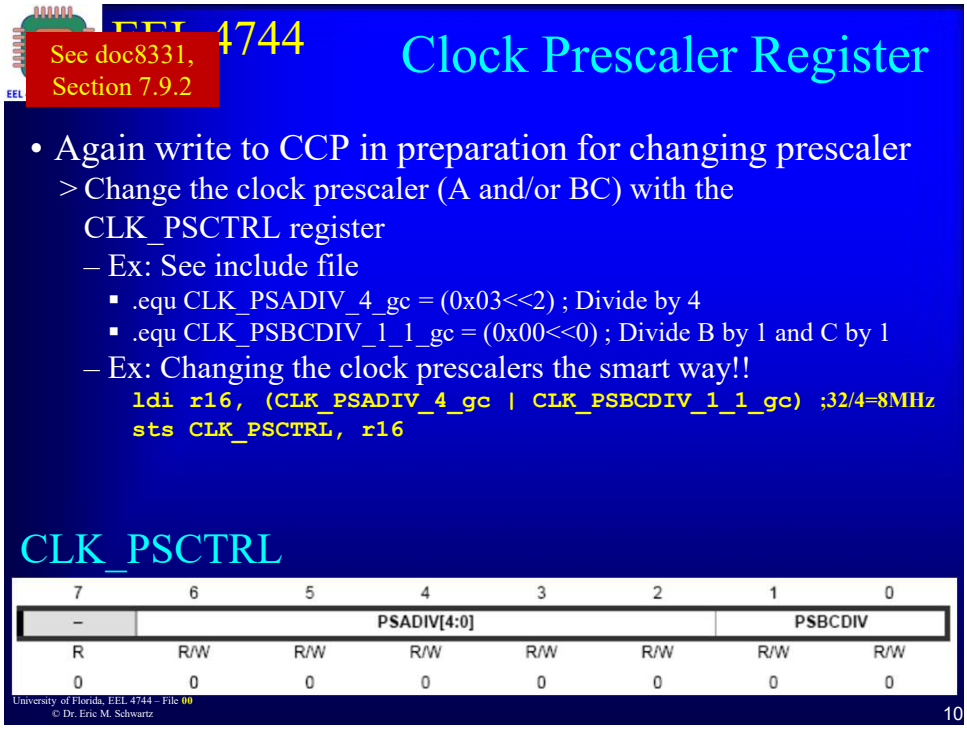

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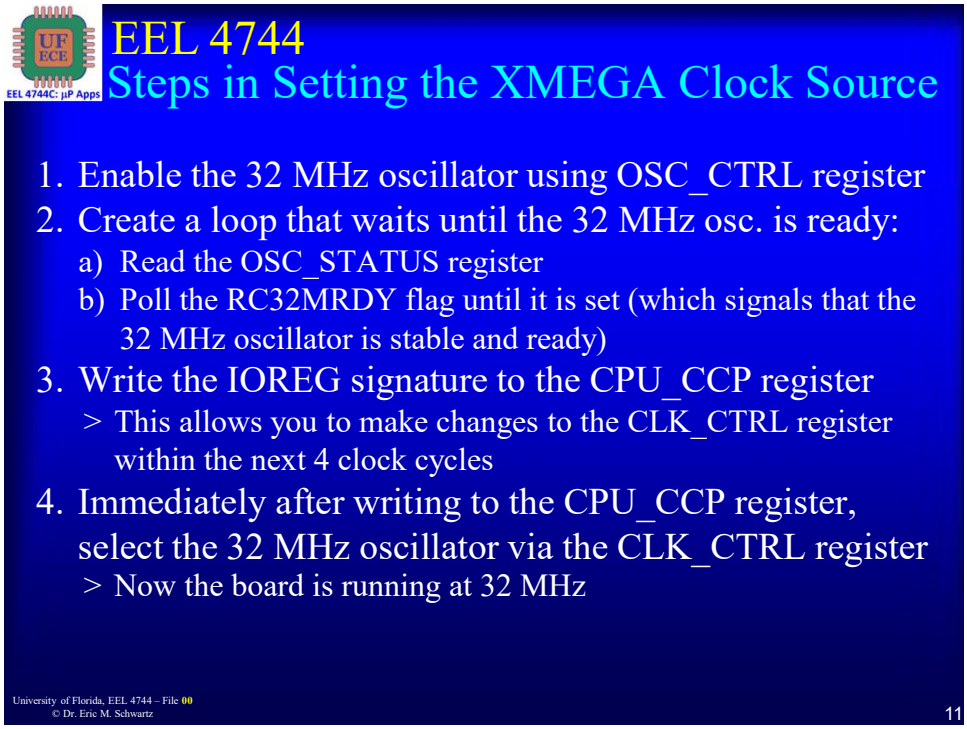
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Steps in Setting the XMEGA Clock Source
1. Enable the 32 MHz oscillator using OSC_CTRL register
2. Create a loop that waits until the 32 MHz osc. is ready:
a) Read the OSC_STATUS register
b) Poll the RC32MRDY flag until it is set (which signals that the 32 MHz oscillator is stable and ready)
3. Write the IOREG signature to the CPU_CCP register
> This allows you to make changes to the CLK_CTRL register within the next 4 clock cycles
4. Immediately after writing to the CPU_CCP register, select the 32 MHz oscillator via the CLK_CTRL register
> Now the board is running at 32 MHz
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Steps in Setting the XMEGA Clock Source
5. If you want to divide the clock speed (slower), again write to CPU_CCP and then to CPU_PSCTRL
> Ex: For 8 MHz, use Prescaler A = 4 and Prescaler BC = 1 & 1
ldi r16, (CLK_PSADIV_4_gc | CLK_PSBCDIV_1_1_gc) ;8MHz
sts CLK_PSCTRL, r16
> See tables 7-2 and 7-3 in doc 8331
> This register is protected by the CCP just like CLK_CTRL, so you must write the IOREG signature to the CPU_CCP register, and THEN write to the CLK_PSCTRL register with your desired clock division configuration
• Summarizing:
> Enable 32 MHz oscillator
> Wait for the oscillator to stabilize
> Select the 32 MHz oscillator as the new clock source
> Divide the clock, if needed
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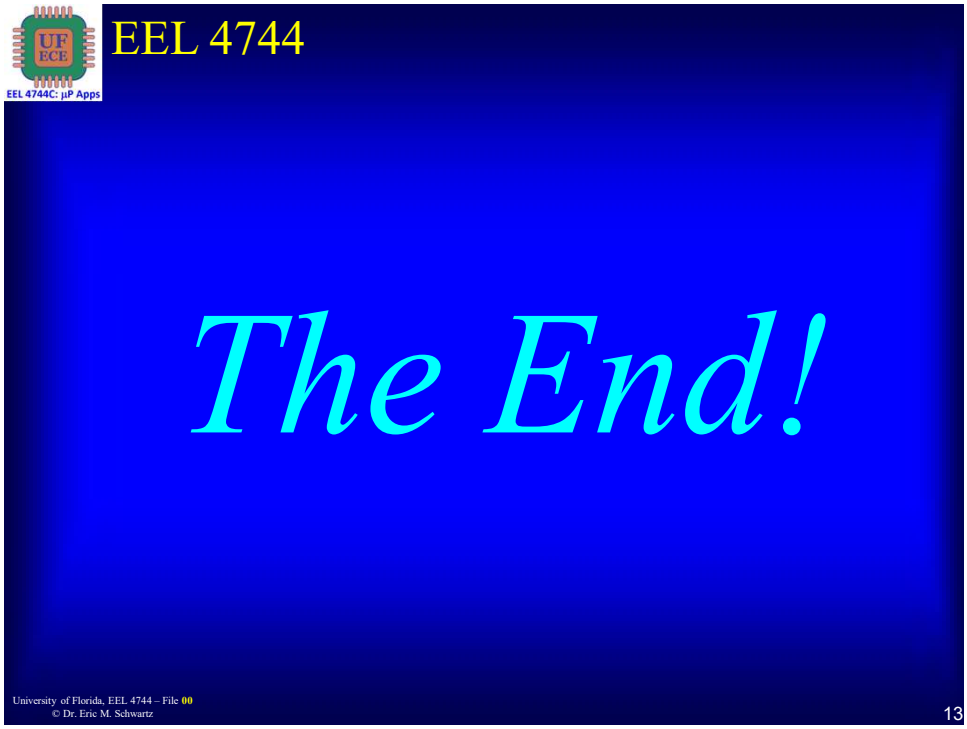
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The End!
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